WHAT IS CLAIMED IS:

1. An equalizer for equalizing a return-to-zero (RZ) signal received from a communication channel, comprising:
   (a) an equalizer core for equalizing the received signal and for updating tap values;
   (b) a decision corrector for detecting and correcting misplaced pulses and double pulses in the equalized signal, wherein the decision corrector:
      (i) comprises a zero assertion counter that generates a clock synchronized with the timing of the received signal, and
      (ii) corrects the equalized signal by forcing zeroes in those portions of the equalized signal that the synchronized clock indicates should be RZ zeroes; and
   (c) an error calculator that generates an error signal based on the outputs of the equalizer core and the decision corrector, and passes that error signal to the equalizer core,

   and wherein the equalizer core updates the tap values based on the error signal received from the error calculator.

2. An equalizer as claimed in claim 1, further comprising:
   (a) interpolators having inputs connected to the output of the equalizer core for generating a plurality of interpolated signals based on the equalized signal;
   (b) a plurality of slicers, each having an input connected to the output of a corresponding interpolator, for comparing the interpolated signal against a threshold value and outputting a signal having:
      (i) a "1" symbol for each portion of the interpolated signal that is positive and has an amplitude exceeding the threshold value,

(ii) a "-1" symbol for each portion of the interpolated signal that is negative and has an amplitude exceeding the threshold value, and

(iii) a "0" symbol otherwise;

(c) a decision combiner having inputs connected to the outputs of the slicers and an output connected to the input of the decision corrector, for combining the output signals of the slicers into a single signal to the decision corrector that includes all "1" or "-1" symbols output by any of the slicers.

3. An equalizer as claimed in claim 2, wherein the interpolators are polyphase filter banks.

4. An equalizer as claimed in claim 1, further comprising a slicer having an input connected to the output of the equalizer core and an output connected to the input into the decision corrector, for comparing the equalized signal against a threshold value and outputting to the decision corrector a signal having:

(a) a "1" symbol for each portion of the equalized signal that is positive and has an amplitude exceeding the threshold value,

(b) a "-1" symbol for each portion of the equalized signal that is negative and has an amplitude exceeding the threshold value, and

(c) a "0" symbol otherwise.

5. An equalizer as claimed in claim 2 or claim 4, further comprising a controller having a peak detector connected to the output of the equalizer core for analyzing the equalized signal, and wherein the controller determines from analysis of the equalized signal the

threshold value to be used by each slicer and passes that threshold value to each slicer.

6. An equalizer as claimed in claim 5, wherein the controller is configured:
   (a) during periods when the peak detector determines the equalized signal from the equalizer core to be stable, to pass to each slicer a constant threshold value; and
   (b) during periods when the peak detector determines the equalized signal from the equalizer core to be unstable, to pass to each slicer a threshold value that tracks the unstable signal.

7. An equalizer as claimed in claim 6, wherein the controller further comprises a hysteresis comparator having an input connected to the output of the peak detector, for controlling transitions between periods when the controller outputs a constant threshold value and periods when the controller outputs a threshold value that tracks the equalized signal.

8. An equalizer as claimed in claim 1, wherein the received signal is a coded RZ signal, and wherein decision corrector further comprises:
   (a) a buffer for storing samples of the equalized signal from consecutive time periods; and
   (b) a misplaced pulse detector for detecting misplaced pulses and double pulses based on the output of the zero assertion counter and the coding in the RZ signal,

   and wherein the decision corrector further corrects the equalized signal by moving the misplaced pulse or doubled portion of the pulse forward or backward in time by moving or zero asserting

samples within the buffer and outputting the results of the modified buffer.

9. An equalizer as claimed in claim 1, wherein the equalizer core is a linear equalizer.

10. An equalizer as claimed in claim 1, wherein the equalizer core is a decision feedback equalizer.

11. An equalizer as claimed in claim 1, wherein the equalizer core uses the least-mean-square algorithm for adapting tap values.

12. An equalizer as claimed in claim 1, wherein the equalizer core uses the RLS algorithm for adapting tap values.

13. An equalizer as claimed in claim 1, further comprising:
   (a) a DC offset estimator having inputs connected to the outputs of the equalizer core and the decision corrector, for estimating a DC offset based on the outputs of the equalizer core and the decision corrector; and
   (b) a DC offset remover having an input connected to the output of the DC offset estimator and an output connected to the input into the equalizer core, for removing the DC offset estimated by the DC offset estimator from the received signal prior to its input into the equalizer core.

14. An equalizer as claimed in claim 1, further comprising an error limiter connected between the error calculator and the equalizer core, for saturating the error signal produced by the error calculator to a predetermined maximum value before the error signal is passed to the equalizer core.

15. A receiver for use in a signal communication system, comprising an equalizer as claimed in claim 1 and further comprising:

(a) an analog-to-digital converter having an output connected to the input into the equalizer, for digitizing the received signal and passing the digitized signal to the equalizer;

(b) a timing error detector having an input connected to a plurality of taps of the equalizer, for measuring group delay and using the measured group delay to determine a timing error for the receiver; and

(c) adjustment circuitry connected between the output of the timing error detector and the analog-to-digital converter, wherein the adjustment circuitry adjusts the timing of the analog-to-digital converter based on the timing error output by the timing error detector.

16. A receiver as claimed in claim 15, further comprising a variable gain amplifier having an output connected to the input into the analog-to-digital converter, for amplifying the received signal prior to its digitization by the analog-to-digital converter.

17. A receiver as claimed in claim 16, wherein the controller is connected to the variable gain amplifier for the controller to calculate and send to the variable gain amplifier a control word selected to ensure that the quantization bit resolution for the analog-to-digital converter is maximized and to maintain the output of the analog-to-digital converter in an optimal range.

18. A receiver as claimed in claim 15, further comprising a signal detector having an input connected to the output of the analog-to-digital converter, wherein the signal detector is connected to send an enable signal to the equalizer on the first incoming "1" or "-1"

symbol after the signal detector detects a signal from the analog-to-digital converter.

19. A method of equalizing a return-to-zero (RZ) signal received from a communication channel, comprising:
   (a) equalizing the received signal;
   (b) generating and synchronizing a clock with the timing of the received signal;
   (c) detecting and correcting misplaced pulses and double pulses in the equalized signal by forcing zeroes in those portions of the equalized signal that the synchronized clock indicates should be RZ zeroes, to produce a corrected signal therefrom;
   (d) calculating a timing error based on the equalized signal and the corrected signal; and
   (e) updating equalizer tap values based on the calculated timing error.

20. A method as claimed in claim 19, further comprising, prior to detecting and correcting misplaced pulses and double pulses in the equalized signal:
   (a) interpolating the equalized signal to produce a plurality of interpolated signals;
   (b) comparing each of the plurality of interpolated signals against a threshold value and outputting a signal having:
      (i) a "1" symbol for each portion of the interpolated signal that is positive and has an amplitude exceeding the threshold value,
      (ii) a "-1" symbol for each portion of the interpolated signal that is negative and has an amplitude exceeding the threshold value, and

(iii) a "0" symbol otherwise; and

(c) combining the plurality of outputted signals into a single signal that includes all "1" or "-1" symbols corresponding to pulses in any of the interpolated signals,

and wherein the detecting and correcting step is performed on this combined output signal.

21. A method as claimed in claim 20, wherein the interpolation is performed using polyphase filter banks.

22. A method as claimed in claim 19, further comprising, prior to detecting and correcting misplaced pulses and double pulses in the equalized signal, comparing the equalized signal against a threshold value and outputting a signal having:

(a) a "1" symbol for each portion of the equalized signal that is positive and has an amplitude exceeding the threshold value,

(b) a "-1" symbol for each portion of the equalized signal that is negative and has an amplitude exceeding the threshold value, and

(c) a "0" symbol otherwise,

and wherein the detecting and correcting step is performed on this output signal.

23. A method as claimed in claim 20 or claim 22, further comprising setting the threshold value based on the measured stability of the equalized signal.

24. A method as claimed in claim 23, wherein:

(a) during periods when the equalized signal is stable, the comparing step proceeds in a constant mode where the

threshold value is set to and remains at a constant value; and

(b) during periods when the equalized signal is unstable, the comparing step proceeds in a tracking mode where the threshold value is adjusted regularly to track the unstable signal.

25. A method as claimed in claim 24 wherein the tracking mode switches to the constant mode when the peaks detected in the equalized signal exceed a predetermined high threshold level, and wherein the constant mode switches to the tracking mode when the peaks fall below a predetermined low threshold level.

26. A method as claimed in claim 19, wherein the received signal is a coded RZ signal, and wherein the detecting and correcting step further comprises:

(a) passing the equalized signal through a buffer;

(b) detecting misplaced pulses and double pulses based on both the synchronized clock and the coding in the RZ signal; and

(c) correcting the equalized signal by moving the misplaced pulse or doubled portion of the pulse forward or backward in time, by moving or zero asserting the samples of the equalized signal in the buffer and outputting the results of the modified buffer.

27. A method as claimed in claim 19, wherein the equalizing step is a linear equalization.

28. A method as claimed in claim 19, wherein the equalizer step is a decision feedback equalization.

29. A method as claimed in claim 19, wherein the equalization step uses the least-mean-square algorithm for adapting tap values.

30. A method as claimed in claim 19, wherein the equalization step uses the RLS algorithm for adapting tap values.

31. A method as claimed in claim 19, further comprising:
   (a) estimating a DC offset based on the equalized signal and the corrected signal; and
   (b) removing the estimated DC offset from the received signal prior to equalizing it.

32. A method as claimed in claim 19, further comprising saturating the timing error to a predetermined maximum value before updating the equalizer tap values based on that timing error.

33. A method as claimed in claim 19, further comprising:
   (a) digitizing the received signal through an analog-to-digital converter prior to equalizing it; and
   (b) adjusting the timing of the analog-to-digital converter based on the group delay indicated by updated tap values.

34. A method as claimed in claim 33, wherein a time constant is selected for adjusting the timing of the analog-to-digital converter that is significantly different from the time constant for the equalization step.

35. A method as claimed in claim 34, wherein the time constants are selected so that adaptation through the equalization step is significantly faster than adaptation through adjusting the timing of the analog-to-digital converter.

36. A method as claimed in claim 33, further comprising amplifying the received signal through a variable gain amplifier prior to digitizing it.

37. A method as claimed in claim 34, further comprising selecting for the variable gain amplifier a control word to maximize the quantization bit resolution for the analog-to-digital converter and to maintain the output of the analog-to-digital converter in an optimal range.

38. A method as claimed in claim 34, further comprising monitoring the output of the analog-to-digital converter, and enabling the equalization step on the first incoming "1" or "-1" symbol after detecting a signal from the analog-to-digital converter.